
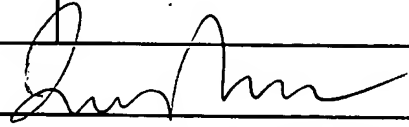


FORM PTO-1449 (REV. 7-80)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. TI-35107	SERIAL NO. Unknown 10/613271		
LIST OF DOCUMENTS CITED BY APPLICANT <i>(Use several sheets if necessary)</i>				APPLICANT Uming Ko, et al			
				FILE DATE Unknown 7/3/03	GROUP Unknown 2816		
U.S. PATENT DOCUMENTS							
*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPROPRIATE)
	AA						
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FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
							YES NO
	AO						
	AP						
	AQ						
	AR						
OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
	AS	S. Shigematsu, et al., "A 1-V High-Speed MTCMOS Circuit Scheme for Power-Down Application Circuits," <i>IEEE Journal of Solid State Circuits</i> , vol. 32, No. 6, pp. 861-869, June 1997.					
EXAMINER 				DATE CONSIDERED 9/9/04			
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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APPLICANT

Uming Ko, et al.

FILE DATE

07/03/03

GROUP

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							YES	NO
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	AQ							
	AR							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AS	"Retention Register for System-Transparent State Retention", U.S. Serial No. 10/616,207, Docket No. TI-34822, Filed on July 3, 2003
AT	
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EXAMINER	DATE CONSIDERED 9/9/04

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